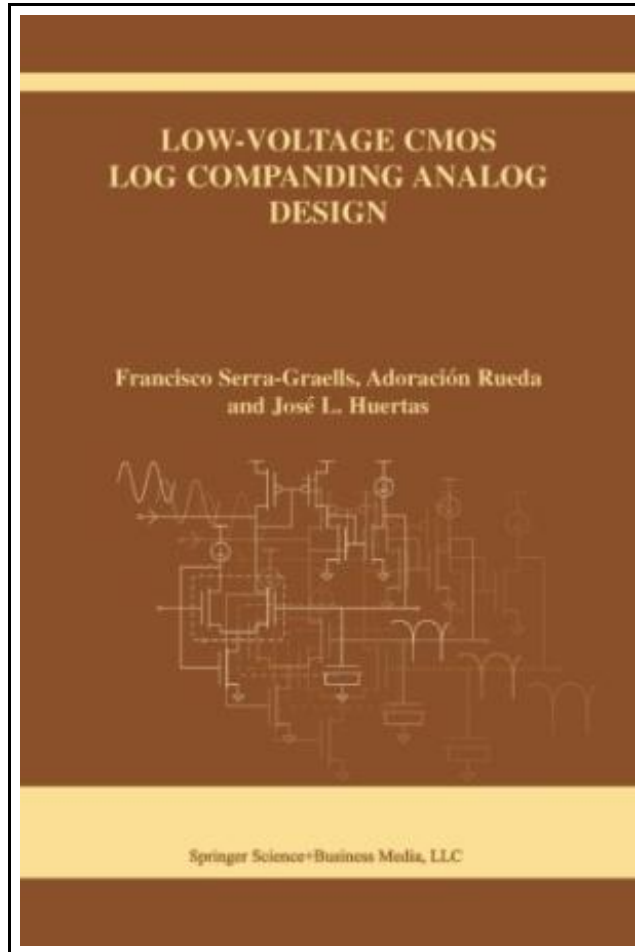


Low-voltage CMOS Log Companding Analog Design



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Reviews

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(Esta Price)*

LOW-VOLTAGE CMOS LOG COMPANDING ANALOG DESIGN



Springer-Verlag New York Inc. Paperback. Book Condition: New. Paperback. 192 pages. Dimensions: 9.2in. x 6.1in. x 0.5in. Low-Voltage CMOS Log Companding Analog Design presents in detail state-of-the-art analog circuit techniques for the very low-voltage and low-power design of systems-on-chip in CMOS technologies. The proposed strategy is mainly based on two bases: the Instantaneous Log Companding Theory, and the MOSFET operating in the subthreshold region. The former allows inner compression of the voltage dynamic-range for very low-voltage operation, while the latter is compatible with CMOS technologies and suitable for low-power circuits. The required background on the specific modeling of the MOS transistor for Companding is supplied at the beginning. Following this general approach, a complete set of CMOS basic building blocks is proposed and analyzed for a wide variety of analog signal processing. In particular, the covered areas include: amplification and AGC, arbitrary filtering, PTAT generation, and pulse duration modulation (PDM). For each topic, several case studies are considered to illustrate the design methodology. Also, integrated examples in 1.2 μ m and 0.35 μ m CMOS technologies are reported to verify the good agreement between design equations and experimental data. The resulting analog circuit topologies exhibit very low-voltage (i. e. 1V) and low-power (few tenths of μ A) capabilities. Apart from these specific design examples, a real industrial application in the field of hearing aids is also presented as the main demonstrator of all the proposed basic building blocks. This system-on-chip exhibits true 1V operation, high flexibility through digital programmability and very low-power consumption (about 300 μ A including the Class-D amplifier). As a result, the reported ASIC can meet the specifications of a complete family of common hearing aid models. In conclusion, this book is addressed to both industry ASIC designers who can apply its contents to the synthesis of very low-power systems-on-chip in standard CMOS...



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